REMARKS

Prior to the present amendment, claims 1-3, 6-8, 11-15 and 18-20 were pending in the application. By the present amendment, claims 6 and 18 have been amended. Thus, after the present amendment, claims 1-3, 6-8, 11-15 and 18-20 remain in the present application. Reconsideration and allowance of outstanding claims 1-3, 6-8, 11-15 and 18-20 in view of the following remarks are respectfully requested.

A. Rejections of Claims 1-3, 6-8, 11-15 and 18-20 under 35 USC §102(e)

The Examiner has rejected claims 1-3, 6-8, 11-15 and 18-20 under 35 USC §102(e) as being anticipated by U.S. Patent Application Publication Number US 2001/0042190 to Tremblay, et al. (hereinafter "Tremblay"). For the reasons discussed below, Applicants respectfully submit that the present invention, as defined by independent claims 1, 7, 11, and 19, is patentably distinguishable over Tremblay.

As disclosed in the present application, conventional approaches in the processor architecture field do not adequately address the problem of consumption of chip area for wide buses, such as wide "move" buses linking various register file banks. Various embodiments according to the present invention address and overcome the need in the art for speeding up the very long instruction word ("VLIW") processor architecture and reducing power consumption and reducing chip area while accommodating multiple register file banks and multiple execution units.

Embodiments according to the present invention, as shown in Figure 2 of the present application, include first and second register file banks. The first register file bank comprises a first plurality of read ports and write ports, and the second register file bank comprises a second plurality of read ports and write ports. A first data path block comprises a first plurality of execution units, and a second data path block comprises a second plurality of execution units. A first plurality of buses couple the first plurality of read ports to each of the first and second data path blocks. A second plurality of buses couple the second plurality of read ports to each of the first and second data path blocks. An operand residing in the first plurality of read ports is concurrently accessed by the first plurality of execution units in the first data path block and by the second plurality of execution units in the second data path block. In addition, a result of an operation performed in the first data path block is written to only the first plurality of write ports of the first register file bank without being written to the second plurality of write ports of the second register file bank.

In the various embodiments of the invention, due to the fact that operands are delivered directly from either register file bank to either data path block, the additional clock cycle required to move an operand from one register file bank to the other register file bank prior to the delivery of the operand to the destination data path block is eliminated. Since operands do not go through move buses 170 and 172 (shown in Figure 1 of the present application), increased speed is achieved due to the elimination of the additional clock cycle existing in a conventional VLIW processor. Moreover, the

charging and discharging of these buses for the purpose of accomplishing a move is avoided, and as such, a substantial power savings is achieved. Thus, by replacing move buses 170 and 172 (shown in Figure 1 of the present application) in a conventional VLIW processor with read buses 260, 262, 264, and 266 in VLIW processor 200 (Figure 2 of the present application), embodiments of the invention achieve increased speed and reduced power without increasing the required chip area.

In contrast, Tremblay is directed to a VLIW processor "having a plurality of functional units and [which] includes a multi-ported register file that is divided into a plurality of separate register file segments." See Tremblay, paragraph 0011, lines 2-4. As seen in Figure 2 of Tremblay, "[a] separate register file segment 224 is allocated to each of the media functional units 220 and the general functional unit 222." See Tremblay, paragraph 0039, lines 6-8. In addition, referring to Figure 6 of Tremblay, separate "register file segments 610, 612, 614, and 616 are partitioned into local registers and global registers." See Tremblay, paragraph 0064, lines 11-12. Whereas the "global registers are read and written by all functional units 620, 622, 624, and 626" (See Tremblay, paragraph 0064, lines 13-14), the "local registers are read and written only by a functional unit associated with a particular register file segment." See Tremblay, paragraph 0064, lines 14-16. Moreover, the global and local registers are considered to be individual and distinct. See, for example, Tremblay, paragraph 0014, lines 1-6.

Tremblay, therefore, does not teach, disclose, or suggest the VLIW processor in the present invention because the register files in Tremblay are divided into individual

local and global registers, which are each written to and accessed by the functional units differently. Accordingly, the disclosure in Tremblay regarding the global registers, which are read *and written to by all* functional units does not teach, disclose or suggest a VLIW processor wherein the result of an operation performed in a first data path block is written to only a first plurality of write ports without being written to a second plurality of write ports as required by independent claims 1, 7, 11, and 19. Furthermore, the disclosure in Tremblay regarding the local registers, which are read *only* by a functional unit associated with a particular register file segment does not teach, disclose or suggest a VLIW processor wherein an operand residing in a first plurality of read ports is concurrently read by a first plurality of execution units in a first data path block and by a second plurality of execution units in a second data path block, as required by independent claims 1, 7, 11, and 19. Thus, the configuration disclosed in Tremblay does not include the efficient bussing architecture included in the present invention. As such, the configuration disclosed in Tremblay does not provide the advantages of increased speed and reduced power, without having to increase the required chip area, as provided by the present invention.

For the foregoing reasons, Applicants respectfully submit that the present invention as defined by independent claims 1, 7, 11, and 19 is not taught, disclosed, or suggested by the art of record. As such, the claims depending from independent claims 1, 7, 11, and 19 are, *a fortiori*, also patentable for at least the reasons presented above and also for additional limitations contained in each dependent claim.

B. Conclusion

Based on the foregoing reasons, the present invention, as defined by independent claims 1, 7, 11, and 19, and the claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing reasons, an early Notice of Allowance directed to claims 1-3, 6-8, 11-15 and 18-20 remaining in the present application is respectfully requested.

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Respectfully Submitted,
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